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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/803,264
Filing Date ..... March 17, 2004
Inventor.....Warren M. Farnworth et al.
Assignee.....Micron Technology, Inc.
Group Art Unit.....2829
Examiner ..... Russell Marc Kobert
Attorney's Docket No. MI22-2524
Title: Method and Apparatus for Testing Semiconductor Circuitry for Operability and Method of Forming Apparatus for Testing Semiconductor Circuitry for Operability

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Reference - - See attached Form PTO-1449

The attached Form PTO-1449 is submitted In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the references listed on the attached Form PTO-1449. Pursuant to Federal Register Vol. 69, No. 182, pg. 56542 (September 21, 2004), no copies of any cited U.S. patents or U.S. published applications are included herewith. Copies of all other cited art references, if any, are attached. No admission is made regarding whether the submitted references are prior art.

Citation of this reference is respectfully requested.

Respectfully submitted,

Date: 8-7-06

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